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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/974,814	10/12/2001	Masashi Sahara	501.40724X00	8257

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EXAMINER
QUACH, TUAN N

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No. 09/974,814	Applicant(s) SAHARA ET AL.	
	Examiner Tuan Quach	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sh et with the correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-70* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-70* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim 67 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 67 is a duplicate of claim 4.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-6, 8-13, 15-20, 22-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamal et al. (hereinafter Kamal).

Kamal teaches a process for self aligned silicidation on a MOS transistor including the argon sputter etch of silicon surface prior to cobalt deposition and

silicidation. The process includes the formation of MOS components including the gate oxide 104, gate 110, source/drain 106/108, sidewall spacers 112/114, conventional HF cleaning, argon sputter etching of silicon oxide on the silicon surfaces, depositing cobalt and effecting silicidation to form silicide contacts on the gate, source, and drain regions. See column 2 line 48 to column 3 line 20, line 59 to column 6 line 48.

The standby current would have been inherent and obvious in the Kamal device, absent evidence to the contrary, given that the same processing is employed in Kamal, including the overlapping native oxide thickness being removed of 20 angstroms, e.g., column 9 lines 1-5, lines 15-18, thus meeting the amount being sputtered etched as in the claims.

The spacer as mask would have been obvious in Fig. 4 or otherwise is notoriously conventional for source/drain implant with the spacer as mask. The configuration of the MOS device to form SRAM memory cell, e.g., as in claim 6, is notoriously conventional and as such would have been obvious and would have been within the purview of one skilled in the art.

Claims 1-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamal in view of Zeininger et al. (hereinafter Zeininger).

Kamal is applied above and further in view of Zeininger wherein the optimization of sputter etching to limit the damage to a few monolayers on the surface of the silicon surfaces would have been further obvious given the teaching of Zeininger, column 2 lines 50-54 wherein the ultra shallow damage region would be obtained for silicidation

and wherein the disadvantages regarding the rough silicides, associated agglomeration, leaky junctions can be obviated.

The spacer as mask would have been obvious in Fig. 4 or otherwise is notoriously conventional for source/drain implant with the spacer as mask. The configuration of the MOS device to form SRAM memory cell, e.g., as in claim 6, is notoriously conventional and as such would have been obvious and would have been within the purview of one skilled in the art.

Regarding the use of same apparatus for sputter etching and metal deposition, e.g, claim 7, such would have been obvious over Kamal in view of Zeininger wherein the same sputtering tool can be employed to effect the sputter etching and sputter deposition, column 2 lines 27-54.

Claims 29-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamal taken with Zeininger.

These claims call for the same processing but recite application in battery-driven in the preamble. Claims 29-33 and 36-40 thus would have been unpatentable over the teachings of Kamal as delineated above wherein all processing steps are met except for the recitation of "battery-driven". The prior art structure however is clearly capable of performing the intended use in battery-driven operations and therefore would meet the claims and wherein the similar process is employed without any structural difference or any manipulative difference as compared to the prior art. Such application into battery-driven device further would have been conventional and well within the purview of one skilled in the art. The configuration of the MOS device to form SRAM memory cell,

e.g., as in claims 34, 41 etc., is notoriously conventional and as such would have been obvious and would have been within the purview of one skilled in the art.

Claims 29-33 and 36-40 would have been further obvious and unpatentable over the combined teachings of Kamal and Zeininger as applied above wherein such optimization of the extent of the sputter etching would have been obvious for the reasons delineated above, namely to form ultra-shallow damage region and to obviate disadvantages such as agglomeration, layer degradation, and leaky junctions.

The use of same apparatus in claims 35 and 42 would have been conventional and obvious for the same reason delineated above in Zeninger, column 2 lines 27-54.

Claims 43-70 are are rejected U.S.C. 103(a) as being unpatentable over Kamal taken with Zeininger, and further in view of Matsubara and Wolf .

Kamal is applied as above singly or in combination with Zeininger teaching the essential processing steps including the sputter etching and further teaches the width of 0.18 micron (column 6 line 62) but does not recite the silicide thickness of 20 to 40 nm.

It would have been obvious to one skilled in the art in practicing the Kamal process to have employed gate width of 0.18 micron or less and silicide thickness between 20 and 40 nm or the silicide with sheet resistance of 5 to 12 ohm per square since such gate dimension and magnitude is contemplated in Kamal and since such is well known in the art as evidenced by Matsubara column 1 lines 10-62 wherein the reduced gate length would result in high density integration and would permit integration with silicide contacts having low resistance; additionally, such silicide thickness optimization would have been obvious and would have been within the purview of one

skilled in the art as delineated in Zeininger, column 3 line 18, in Matsubara column 1 lines 57-60, and in Wolf, page 151 fifth paragraph. The selection and optimization of sheet resistance of including of 5 to 12 ohm per square would have conventional and obvious and would have been within the purview of one skilled in the art and as evidenced by the teaching references wherein silicide contacts having low resistance are obtained as delineated above and further in Wolf, page 151, fifth paragraph.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Shields is cited of interest.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Quach whose telephone number is 703-308-1096. The examiner can normally be reached on M - F from 9 to 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Wael Fahmy can be reached on (703) 308-4918. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9318 (Before Final) and (703) 872-9319 (After Final).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Tuan Quach
Primary Examiner